(12) Patent Laid-open Official Gazette (A)
(19) Japanese Patent Office (JP)
(11) Patent Laid-open No. **Sho 60-245174**
(43) Date of Laid-open: December 4, 1985

(51) Int. Cl.[4]
H 01 L 29/78
H 01 L 21/324

Discrimination Mark:
Official Reference Number:
8422-5F
6603-5F

Request for Examination: Yes
Number of Invention: 1

(Total: 5 pages)

(54) Title of Invention:
Manufacturing method of insulated gate type field effect semiconductor device

(21) Patent Application No. Sho 59-100252
(22) Filing Date: May 18, 1984

(72) Inventor: Shunpei Yamazaki
c/o Semiconductor Energy Laboratory, Co., Ltd.
21-21, 7-chome Kitakarasuyama, Setagaya-ku, Tokyo

(71) Applicant: Semiconductor Energy Laboratory, Co., Ltd.
21-21, 7-chome Kitakarasuyama, Setagaya-ku, Tokyo

SPECIFICATION

1. TITLE OF INVENTION

Manufacturing method of insulated gate type field effect semiconductor device

2. CLAIMS

1. Manufacturing method of an insulated gate type field effect semiconductor device comprising the steps of:

forming a non-single crystal semiconductor added with hydrogen or halogen elements on a substrate;

forming a gate insulating film on said semiconductor;

selectively forming a gate electrode on said insulating film;

adding an impurity for P or N type to said non-single crystal semiconductor utilizing said gate electrode as a mask; and

promoting crystallization of a region added with impurity after said process by a strong light irradiation.

2. The manufacturing method of an insulated gate type field effect semiconductor device of Claim 1 wherein the impurity for P or N type is added through the gate insulating film, and said gate insulating film constitutes a film for preventing deairing of hydrogen or halogen elements during the strong light irradiation.

3. DETAILED DESCRIPTION OF THE PRESENT INVENTION

"Field for Industrial Use"

The present invention relates to an insulated gate type field effect semiconductor device (hereinafter referred to as IGF) utilized for a semiconductor integrated circuit, a liquid crystal display panel, and the like.

"Prior Art"

IGFs utilizing single crystal silicon are widely utilized in the field of semiconductors. A typical example is Japanese Patent Pub. No. Sho 50-1986 "SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" invented by the present inventor. However, with regard to IGF whose channel formation region not added with hydrogen is not made of a single crystal semiconductor, but made of a non-single crystal semiconductor added with hydrogen or halogen elements at a concentration of 1 atom% or more, a typical example is shown in Japanese Pat. Appl. No. Sho 53-124021 "SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" invented by the present inventor (filed on October 7, 1978).

This IGF whose channel formation region comprises a semiconductor, especially a silicon semiconductor added with hydrogen or halogen elements, has OFF-state current of $1/10^3$ to $1/10^5$ of that of the conventional IGF utilizing a single crystal semiconductor. Therefore it is believed that this IGF is used effectively for controlling a liquid crystal display panel. As in the example above mentioned, there are three types of semiconductors as this IGF: there are a lateral channel type IGF wherein a gate electrode is formed on a semiconductor of a channel formation region, a vertical channel type IGF mentioned in Japanese Pat. Appl. No. Sho 56-001767 "INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" by the present inventor (January 9, 1981), and a conventional thin film IGF transistor type wherein a gate electrode is provided beneath a semiconductor composing a channel formation region. Compared with the latter two, the structure of the former is the same as that of the conventionally known IGF utilizing single crystal silicon. Thus this IGF has a superiority that established technologies can be applied.

However, a source and a drain of this IGF should be formed not through a CVD method (including a plasma CVD method) by deposition

of a thin film, but through ion implantation, etc. Donors and acceptors have to be activated by annealing under a temperature of 400 °C or less, which is the range hydrogen or halogen elements are not deaired.

From this point of view, aforementioned patent applications by the present inventor are not necessarily clear.

"Means to Solve the Problems"

The present invention aims to solve the problems above mentioned. A gate insulator and a gate electrode above it are selectively formed on a non-single crystal semiconductor with no or little doped impurities (hereinafter non-single crystal semiconductor added with hydrogen or halogen elements is simply referred to as a semiconductor, or a non-single crystal semiconductor). Utilizing this gate electrode as a mask, impurities for the source and the drain are added by an ion implantion method or the like. For example, phosphorous or arsenic is added for N channel type, and boron is added for P channel type, into the non-single crystal semiconductor through the gate insulating film. After that, strong light is irradiated at 400 °C or less to the regions added with these inactive impurities, thereby performing strong light anneal (hereinafter simply referred to as light anneal). Added hydrogen or halogen elements are retained by blocking of the gate insulating film, and the semiconductor is transformed into a semiconductor with crystallinity promoted more than that of the channel formation region, particularly a semiconductor having a polycrystal or single crystal structure.

In the conventionally known method, after ion implantation is performed, laser anneal is performed to single crystal silicon with no hydrogen nor halogen elements added. Unlike the conventionally known method, ion implantation, then strong light anneal are performed to a non-single crystal semiconductor with hydrogen or

halogen elements added at a concentration of 1 atom% or more, generally 5 to 20 atom%, preferably this light is scanned from one end to the other end of the substrate. Thus crystal growth is to be a part of the processes, crystallinity is promoted, and impurity regions are formed.

"Results"

As a result, in the structure of the IGF of the present invention, a gate electrode is provided on or above the non-single crystal semiconductor composing a channel formation region on a substrate. In addition, an active impurity region with optical Eg of 1.6 eV to 1.8 eV, which is almost the same as the optical Eg (1.7 to 1.8 eV in the case of a silicon semiconductor) of this semiconductor is obtained. Since Eg is the same as or approximately the same as that of the channel formation region, ON-state current flows smoothly at rise time, and OFF-state current will not likely to flow sluggishly at fall time. In other words, OFF-state current is less and ON/OFF can be switched with high speed response.

The present invention is explained according to the following embodiment.

"Embodiment 1"

As shown in Fig.1 (A), a quartz glass substrate of 10 cm x 10 cm large and 1.1 mm thick is utilized as a substrate (1). A non-single crystal semiconductor (2) including an amorphous structure added with hydrogen at a concentration of 1 atom% or more is formed in a thickness of 0.2 μ by a photo CVD method (low pressure mercury lamp including a wavelength of 2537 Å and a substrate temperature of 210℃) without utilizing mercury enhancing method of disilane(Si_2H_6). A silicon nitride film (3) is deposited thereon as a gate insulating film by a photo CVD method without having the semiconductor surface

exposed to the air in the same reaction chamber. That is, Si_3N_4 is formed in a thickness of 1000 Å by a reaction of Si_2H_6 with ammonia or hydrazine (a low pressure mercury lamp including a wavelength of 2537 Å and a substrate temperature of 250 °C) without utilizing a mercury enhancing method.

Then portions other than a region (5) composing an IGF are removed by a plasma etching method. This reaction is performed as $CF_4 + O_2$ (5%) at 13.56 MHz at a room temperature. A microcrystal or polycrystal semiconductor of N^+ conductivity type is deposited in a thickness of 0.3 μ on this gate insulating film. This N^+ semiconductor film is removed utilizing a resist (6) by a photoetching method. Then phosphorous is added to the regions to be a source and a drain utilizing this resist and an N^+ semiconductor gate electrode portion (4) as masks by an ion implantion method at a concentration of 1×10^{20} cm^{-3}, as shown in Fig.1 (B). Thus a pair of impurity regions (7) and (8) are formed.

After the resist of the gate electrode is removed, strong light (10) anneal is performed on the whole substrate. That is, light is irradiated in a linear shape utilizing an extra-high pressure mercury lamp (output of 5 KW, wavelength of 250 to 600 nm, diameter of 15 mmϕ, length of 180 mm) having a parabolic reflection mirror at its back side and a quartz cylindrical lens (focal distance of 150 cm, converging width of 2 mm, length of 180 mm) in its front. The irradiated part of the substrate is scanned at a speed of 5 to 50 cm/min. to have strong light irradiate to the entire surface of the substrate of 10 cm x 10 cm. Because a large amount of phosphorous has been added to the gate electrode portion, this electrode absorbs enough light and polycrystallizes itself. The impurity regions (7) and (8) once dissolve and recrystallize. They dissolve in the direction of scanning, that is, in the direction of X. Recrystallization is shifted (transferred). As a result,

compared with the case of merely heating or irradiating the entire substrate evenly, grain size of crystals can be made bigger because a system of crystal grain growth has been added.

It is not at all imperative that the regions polycrystallized by this strong light anneal reach the entire region under the impurity regions. As shown in broken lines (11) and (11') in the figure, what is important is that only the portions above these are at least crystallized and the impurities are activated. Ends (15) and (15') of these portions are provided in the channel more inward than the ends (16) and (16') of the gate electrode. N (7), (8) - I (2) junction interface (17) and (17') are provided inside of the crystallized region, and the channel formation region is provided in a hybrid structure by utilizing a non-single crystal semiconductor of an I type semiconductor and a crystal semiconductor. The level of the crystallized semiconductor region in the I type semiconductor can be determinded by scanning speed and intensity (the level of irradiation) of light anneal.

In the figure, after the process in Fig.1 (B), PIQ is coated on the whole surface in a thickness of 2 μ, and formed as electrode holes (13) and (13'), then as ohmic contact of aluminum and its leads (14) and (14'). In the process of forming these (14) and (14') being a second layer, they can be connected with the gate electrode (4).

As a result of this light anneal, sheet resistance changed from 4×10^{-3} $(\Omega cm)^{-1}$ before light irradiation to $1 \times 10^{+2}$ $(\Omega cm)^{-1}$. This change in the electric conductivity characteristic is clearly shown.

Under the condition that the lengths of the channel formation regions are 3 μ and 10 μ and a channel width is 1 mm, as shown in Fig.2 (21) and (22) respectively, electric current of 1×10^{-5} A, 2×10^{-5} A is obtained under V_{th} = +2 V, V_{DD} = 10 V. OFF-state current is (V_{GG} = 0 V) 10^{-10} to 10^{-11} (A), which is $1/10^{-4}$ of 10^{-6} A of a single crystal semiconductor.

"Effects"

Because the present invention utilizes the manufacturing process of forming and processing films gradually from lower levels, large-area large-scale integration is realized. Therefore as many as 500 x 500 pieces of IGFs can be formed in a 30 cm x 30 cm panel, and can be utilized as IGFs for controlling liquid crystal display elements.

Because low-temperature process at 400 °C or less by light anneal process is utilized, a polycrystallized or single crystal semiconductor can be prevented from emitting hydrogen or halogen elements inside it.

Moreover, light anneal is not performed to the entire substrate at a time but is scanned from one end to the other end. For this purpose, light from a cylindrical extra-high pressure mercury lamp is condensed by the use of a parabolic mirror and a quartz lens to form linear light. By scanning the substrate perpendicular to this light, light anneal to the surface is performed.

As this light anneal utilizes ultraviolet rays, crystallization from the surface of the semiconductor to the portion inside is promoted. Thus electric current flowing through the channel formation region near the gate insulating film to the fully polycrystallized or single-crystallized impurity regions near the surface can be controlled with no problem.

Single crystal semiconductors are not at all utilized as substrates. Thus hydrogen or halogen elements added to the channel formation region can keep the state of a non-single crystal semiconductor without being influenced by the light irradiation anneal process. Therefore OFF-state current can be made $1/10^3$ to $1/10^5$ of that of a single crystal semiconductor.

Because the source and the drain are formed by light anneal after formation of the gate, the interface of the gate insulator will not be contaminated and its characteristic is stable. Unlike

the conventional method, not only quartz glass but also soda glass, and a heat endurable organic film can be utilized as optional substrate materials.

The formation of a semiconductor - a gate insulator - a gate electrode comprising a channel formation region of interfaces of different materials and the processes in the same reaction chamber can be performed without being exposed to the air. Thus it is characterized in that interface traps are rarely generated.

In the present invention, it is preferable that each impurity concentration of oxygen, carbon and nitrogen in the non-single crystal semiconductor of the channel formation region is 1×10^{18} cm^{-3} or less. In the conventionally known IGF, impurities are mixed in the channel layer at a concentration of 1 to 3×10^{20} cm^{-3}. In the case of utilizing an amorphous silicon semiconductor, life time of carriers, especially that of holes, are shortened. Thus, in terms of characteristics, current flown is as little as 1/3 or less of that of the present invention. In addition, hysteresis characteristic is observed when drain electric field is applied at 2×10^{6} V/cm or more to I_{DD} - V_{GG} characteristic. On the other hand, when oxygen is 5×10^{18} cm^{-3} or less, hysteresis is not observed even with an electric potential of 3×10^{6} V/cm.

4. BRIEF DESCRIPTION OF THE FIGURES

Fig.1 shows cross sectional views of the manufacturing processes of the insulated gate field effect semiconductor device of the present invention.

Fig.2 shows characteristic of drain current - gate voltage.

Applicant
Semiconductor Energy Laboratory, Co., Ltd.
Representative: Shunpei Yamazaki